CLAIMS

1. A leadframe for a semiconductor device, the leadframe comprising:

a paddle ring having an inner perimeter, an outer perimeter, and a cavity located within the inner perimeter for receiving an integrated circuit die;

a first row of terminals generally surrounding the paddle ring outer perimeter; and

a second row of terminals surrounding the first row of terminals.

2. The leadframe of claim 1, wherein the outer perimeter of the paddle ring includes a plurality of spaced projections.

3. The leadframe of claim 2, wherein the inner perimeter of the paddle ring also includes a plurality of spaced projections.

4. The leadframe of claim 1, further comprising a paddle flag member located within the cavity that supports the integrated circuit die.

5. The leadframe of claim 4, wherein the flag member is integral with the paddle ring.

6. The leadframe of claim 1, wherein each of the terminals of the first row of terminals is individually connected to the paddle ring.

7. The leadframe of claim 6, wherein each of the terminals of the second row of terminals is connected to one side of a connection bar.

8. The leadframe of claim 7, wherein the paddle ring is generally square shaped and the connection bar is connected to at least one of the terminals of the first row of terminals or the paddle ring at a corner thereof.

9. The leadframe of claim 8, wherein another row of terminals is connected to the other side of the connection bar, said another row of terminals for connecting to a second integrated circuit die.

10. The leadframe of claim 1, wherein the leadframe is formed of copper.

11. The leadframe of claim 10, wherein the leadframe is formed via an etching process.

12. A semiconductor device, comprising:

a paddle ring having an inner perimeter, an outer perimeter, and a cavity located within the inner perimeter;

a first row of terminals generally surrounding the paddle ring outer perimeter;

a second row of terminals surrounding the first row of terminals; and

an integrated circuit die placed within the cavity and surrounded by the paddle ring, the die including a plurality of die pads that are electrically connected to respective ones of the terminals of the first and second rows of terminals.

13. The semiconductor device of claim 12, further comprising:

a flag member located within the cavity that supports the integrated circuit die; and

an adhesive material layer disposed on a top surface of the flag member for securing the die to the flag member.

14. The semiconductor device of claim 13, wherein the flag member is integral with the paddle ring.

15. The semiconductor device of claim 12, further comprising an encapsulant covering a top surface of the integrated circuit die, the first and second rows of terminals, and the paddle ring, wherein at least a bottom surface of the first and second rows of terminals is exposed.

16. The semiconductor device of claim 12, wherein the inner perimeter of the paddle ring includes a plurality of spaced projections.

17. The semiconductor device of claim 16, wherein the outer perimeter of the paddle ring also includes a plurality of spaced projections.

18. A method of packaging a semiconductor device comprising the steps of:

forming a leadframe having a paddle ring including an inner perimeter, an outer perimeter and a cavity located within the inner perimeter, a first row of terminals surrounding the paddle ring and individually connected thereto, and a second row of terminals surrounding the first row of terminals, wherein the terminals of the second row of terminals are connected to a connection bar and the connection bar is connected to

at least one of the terminals of the first row of terminals and the paddle ring;

placing an integrated circuit die within the cavity;

electrically connecting die pads of the integrated circuit die to the terminals of the first and second rows of terminals;

performing a first singulation operation that separates the terminals of the first row from the paddle ring; and

performing a second singulation operation that separates the terminals of the second row from the connection bar and separates the connection bar from the connected one of the at least one of the terminals of the first row of terminals and the paddle ring.

19. The method of packaging a semiconductor device of claim 18, further comprising the step of forming a mold compound over a top surface of the integrated circuit die, the electrical connections connecting the die pads of the integrated circuit die to the terminals of the first and second rows of terminals, and a top surface of the first and second rows of terminals.

20. The method of packaging a semiconductor device of claim 19, further comprising the step of performing a molding process after the electrical connecting step and before the first and second singulation operations.

21. The method of packaging a semiconductor device of claim 19, wherein a bottom surface of the first and second rows of terminals is exposed.

22. The method of packaging a semiconductor device of claim 19, wherein the electrical connections are made by performing a wirebonding process.